PERFORMANCE IMPROVEMENT OF FRACTIONAL ORDER PLL

[1]S. Jena, [2]S. Swain*, [3]M. C. Tripathy, [4]S. Behera

[1]M. Tech, Department of E&I, College of Engineering and Technology. Bhubaneswar.

[2]Ph.D. Scholar, Department of E&I, College of Engineering and Technology. Bhubaneswar.

[3]Assistant Professor, Department of E&I, College of Engineering and Technology. Bhubaneswar.

[4]Professor, Department of E&I, College of Engineering and Technology. Bhubaneswar.

Abstract: *Assemble of Phase Locked Loop (PLL) in Fractional domain is the main objective of this paper. At the beginning basics of Fractional Calculus and Phase Locked Loop is readdressed. The fractional order PLL consists of a low-pass filter, a phase detector and a VCO. The MATLAB SIMULINK and LabVIEW models of both integer and fractional order PLL are analyzed. The modelling of fractional order PLL is organized by means of control modelling blocks in Laplace domain. Time domain analysis is also carried out for fractional order PLL by varying α and β values. It has been observed that lower fractional order PLL's will require lesser time to reach the required phase as compared to their integer counterparts. Then stability analysis is done by plotting the complete analysis using Nyquist plots.*

Keywords: **Fractional order, Low pass filter, Phase Locked Loop, Stability, Phase detector, VCO.**

1. INTRODUCTION

Phase-locked loops (PLLs) are a set of regulation systems. PLLs are used to maintain coherence between the output frequency (f_o) and the input frequency (f)) by comparing the phase between the two [1]. The basic PLL system consist of three basic parts; a VCO, phase detector (PD), and low pass filter (LPF) within its loop. It finds wide range applications in AM and FM demodulator circuit, FSK decoders, motor speed control systems, pulse wave synchronization in TV sets and RADAR systems and frequency synthesis [2]. It finds wide applications in frequency multiplier, demodulator circuit, tracking generator, and clock recovery circuit [3]. PLL is often used to suppress unwanted frequency or phase fluctuations in locked oscillator. It is also used in communication equipment, computers, and televisions. The conventional PLL has integer order or classical capacitors in the loop filter and VCO and is called an integer-order PLL. Contrastingly, fractional-order PLL (FPLL) refers to the case where either or both the capacitors are replaced by fractional capacitor(s). FPLL trounces its integer-order counterpart even in the presence of noise. The bandwidth of FPLLs increased as the loop fractional order decreases

which improved both the loop capturing time and locking range. Notwithstanding, the increase in the FPLL bandwidth makes it susceptible to internal and external noise [4]

The perceptions of fractional order elements were first familiarized in 1941 by Cole brothers for demonstration of dielectrics, where $z_F = \frac{R}{c\,\tilde{s}}$ where R is a constant of unit Ω and τ of unit second and z is the fractional number. In literature, many researchers favor fractional order elements such as Fractional capacitor. A passive element having a phase angle between 0° to -90° and being independent of frequency is termed as fractional capacitor. The fractional capacitor's impedance is given by [5-7],

$$Z = \frac{1}{C_F.S^{\alpha}} = \frac{1}{C_F.\omega^{\alpha}} \angle \frac{\pi\alpha}{2} \tag{1}$$

Now a day's consideration is drawn towards the use of fractional calculus in the grounds of control systems, signal processing, electrical circuits, electromagnetics etc. [8-12]. The arrival of fractional order devices (FODs), which created interest among researchers to study its behavior and effect in fractional order circuits and systems. The fractional order circuits are best modelled by fractional calculus in the form of fractional derivatives and integrations [6]. So, the fractional integration of αth order of the function f (t) is defined as,

$$J^{\alpha}(t) = \frac{1}{(\alpha)_0} \int (t-r)^{\alpha-1} f(r)dr \tag{2}$$

The Laplace Transform of the fractional Integral is

$$\{J^{\alpha} f(t)\} = S^{-\alpha} F(s) \tag{3}$$

Here, F(s) is the Laplace transform of (t)

2. ANALYSIS OF FRACTIONAL ORDER PLL

The conventional PLL has integer order or classical capacitors in the loop filter and VCO and is called an integer-order PLL. Contrastingly, fractional-order PLL (FPLL) refers to the case where either or both the capacitors are replaced by fractional capacitor(s). A fractional-order PLL can be realized by using either a fractional-order loop filter (FLF) or a fractional voltage-controlled oscillator (FVCO) or both in the basic PLL structure. The FLF or FVCO can be constructed either by using a R-C ladder network or by using a RC-Symmetric constant phase element known as fractional capacitor. The performance of the FPLL is controlled by the order of the fractional capacitors α and β in the loop filter ($0 < \alpha < 1$, $0 < \beta \leq 1$). Conventional integer-order PLL with $\alpha = \beta = 1$ is a special case of the FPLL.[13]

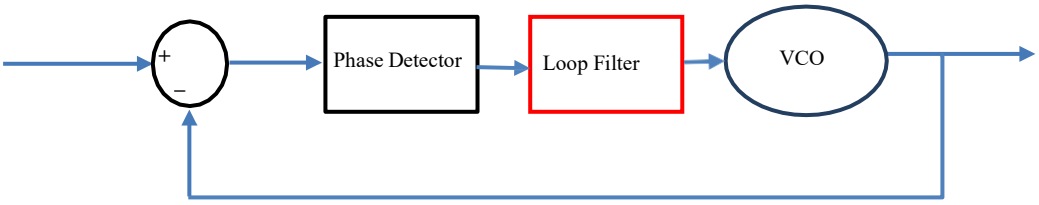


Figure 1. Block diagram representation of Phase Locked Loop (PLL).

The Voltage Controlled Oscillator (VCO) generates a clean waveform to track the frequency and phase of the input signal. The input signal may contain noise also. In order for the correct estimation of the phase of the input signal the error between two signals should be minimum. The error between two signals will be minimized by Low Pass Filter whose output controls the VCO output [14]. The characteristic polynomial of FPLL is obtained from the transfer functions of fractional-order LF and Integer-order VCO.

Here a two-stage loop filter is designed by cascading two 1st order fractional low pass filters.

The integrator $\frac{1}{S}$ when connected to a power function it becomes $\frac{1}{S^{\alpha}}$ and by adding unit feedback gain it becomes $\frac{1}{1+S^{\alpha}}$. Similarly, another fractional order low pass filter of order β is designed and by cascading two low pass filters we got a two-phase loop filter of transfer function expressed as

$$T_{FLPF} = \frac{V(S)}{V_i(S)} = \left(\frac{K_{\alpha}}{a+S^{\alpha}}\right)\left(\frac{K_{\beta}}{b+S^{\beta}}\right) \quad (4)$$

Where $K_{\alpha}$and K_{β} are the sensitivity of the loop filter, and α and β are the order of fractional LF.

Similarly, the transfer function of a integer-order VCO can be expressed as

$$T_{VCO} = \left(\frac{K_0}{S}\right) \quad (5)$$

Where K_0 in $\left(\frac{adian/sec}{volts}\right)$ is called VCO sensitivity.

The relation between input signal phase and VCO output phase can be expressed by the following transfer function

$$\frac{\theta_O(S)}{\theta_i(S)} = \frac{K}{S(a+S^{\alpha})(b+S^{\beta})+K} \quad (6)$$

Where, θ_O is the output phase of VCO

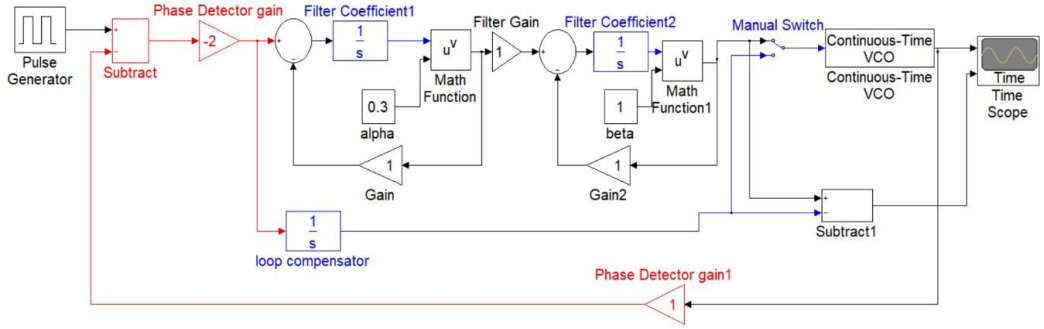
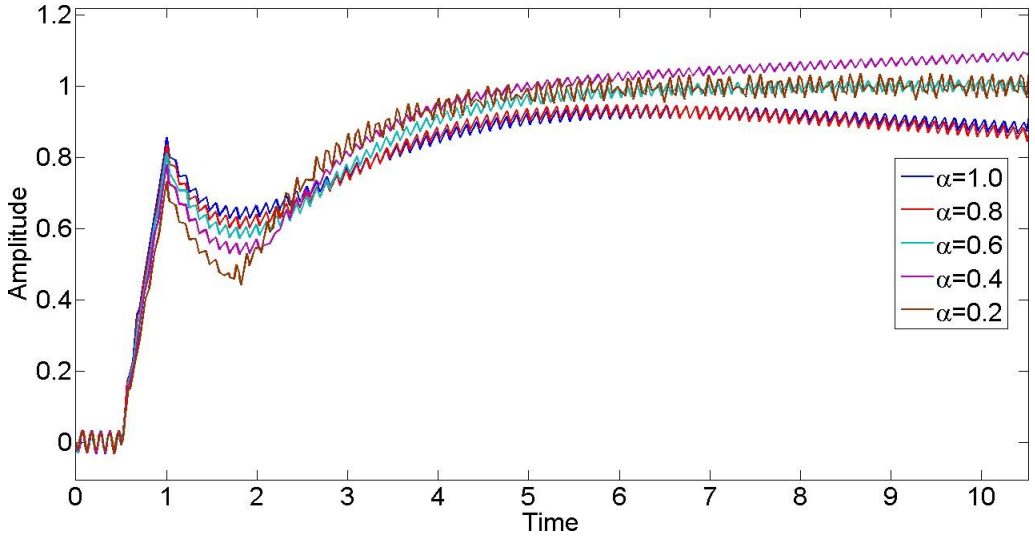
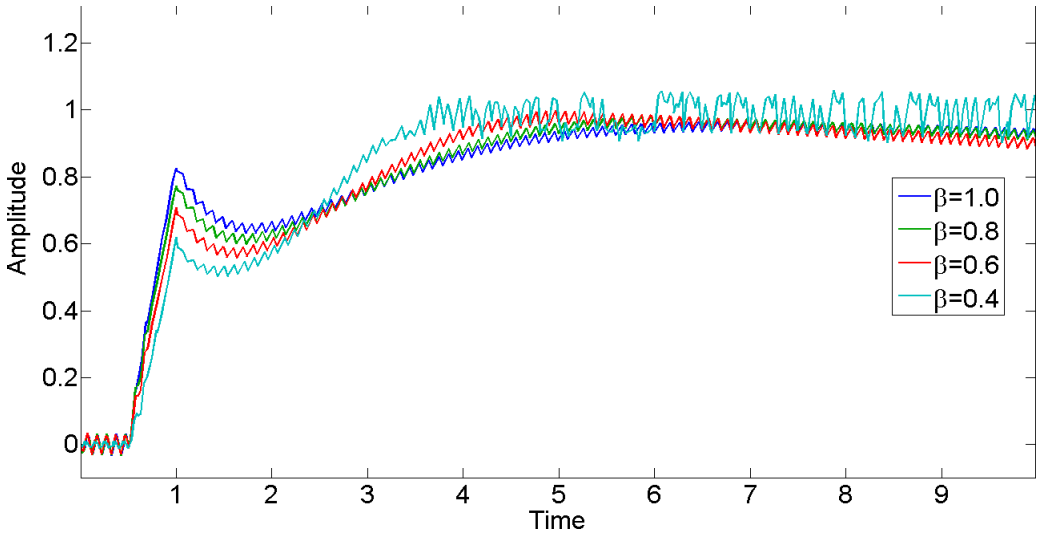


Figure 2. MATLAB Simulink model of 2 stage Fractional-order Phase Locked Loop.

Here, the fractional order PLL is modelled in MATLB Simulink by making use of controlled modelling method by virtue of which the power fraction of the laplace operator 1/s is raised to α i.e., the fractional value.



(a)



(b)

Figure 3. Time domain analysis of Fractional order PLL Circuit with (a) varying α order and (b) varying β order.

The Figure.3 shows the behavior of the fractional order PLL at varying orders of α and β, here it enables the procedure and functions which shows the variety of response at different orders of PLL.

Table.1. Step analysis of fractional order PLL at varying orders α.

Fractional Orders	Maximum peak (degrees)	peak time (n sec)	Settling time (n sec)
α = 1.0	1	0.82	6
α = 0.8	1	0.81	5
α = 0.6	1	0.8	4.5
α = 0.4	1	0.72	4.4
α = 0.2	1	0.7	5

The Table. 1 show that at α=0.4, the Fractional order PLL performs best. It produces a settling time of 4.4 which is minimum in all other fractional orders. Though a peak of 0.72 is experienced in this fractional order, but it is acceptable in comparative analysis.

Table.2. Step analysis of fractional order PLL at varying orders β.

Fractional Orders	Maximum peak (degrees)	peak time (n sec)	Settling time (n sec)
β = 1.0	1	0.81	7
β = 0.8	1	0.79	6.5
β = 0.6	1	0.7	6
β = 0.4	1	0.61	6

From the above tables it has been found that the maximum peak and settling time gradually decreased when the value of α and β decreased as comparison to the conventional basic PLL however the peak time remains same in all the cases.

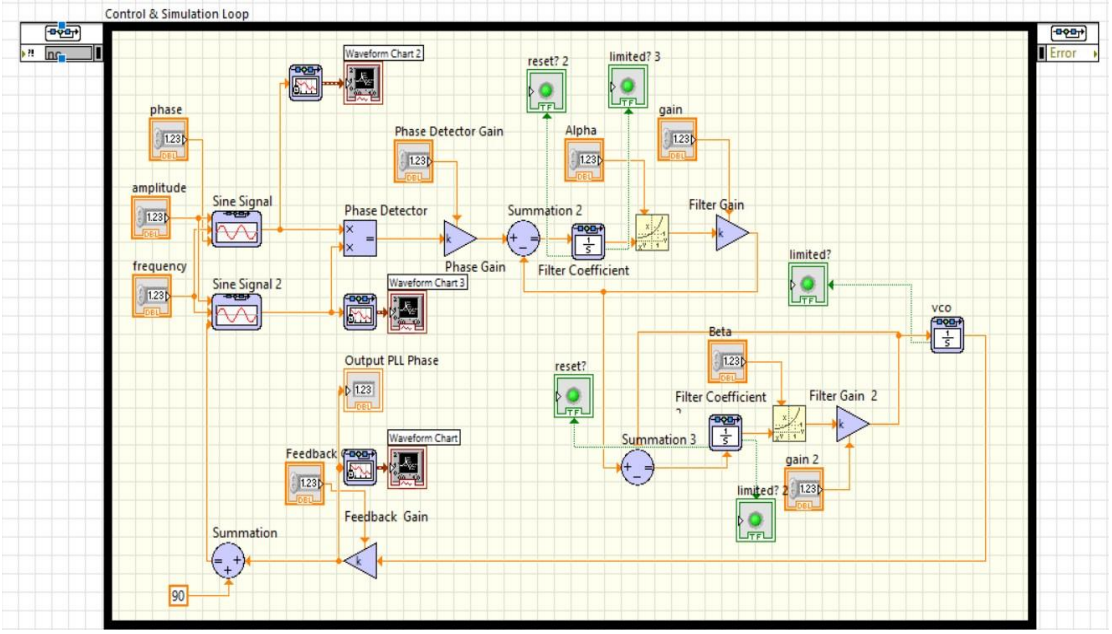
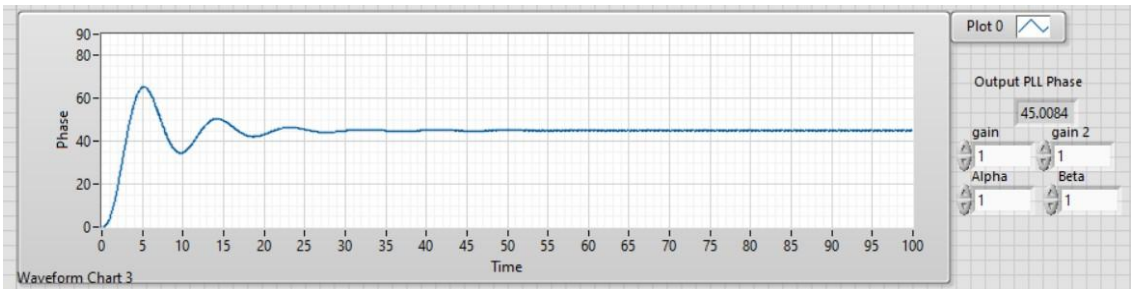
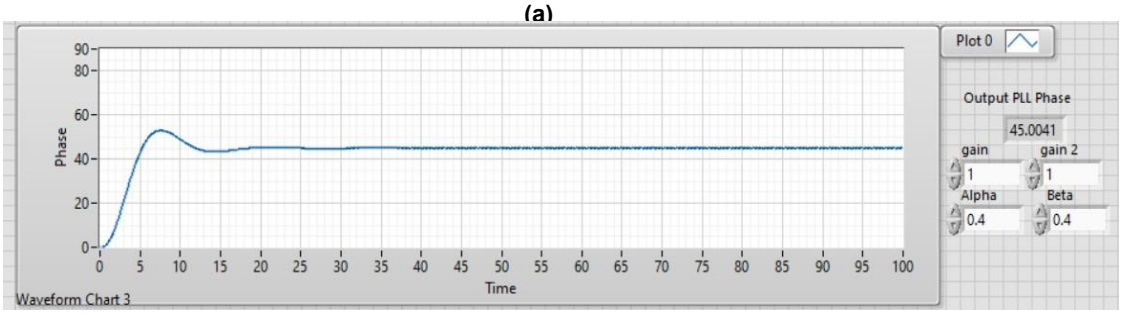


Figure 4. Lab-VIEW model of Fractional-order Phase Locked Loop.

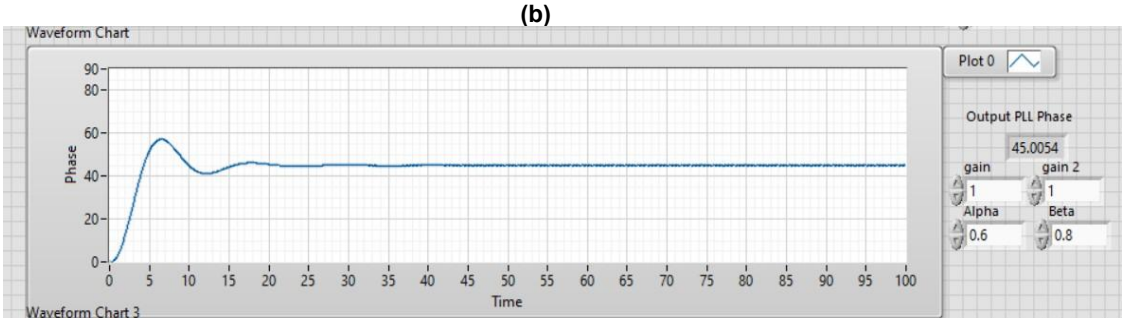
The control design of fractional order PLL is modelled in LABVIEW and two FLFs are designed using two FCs of order of α and β. The output of VCO has been given to thr PD as input till the phase lock is achieved.



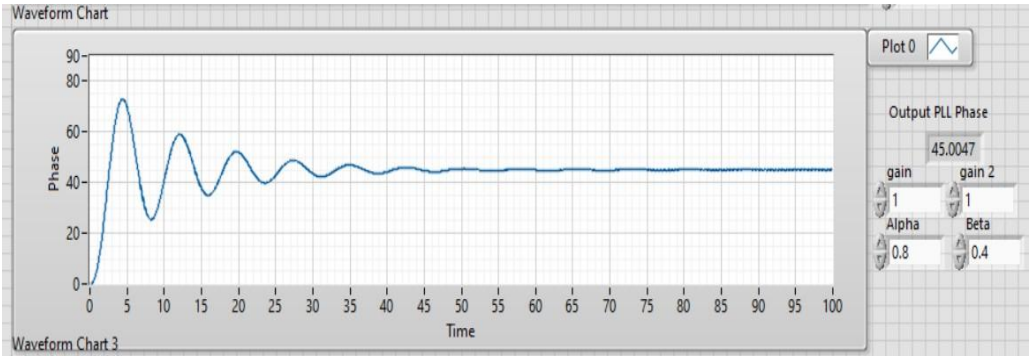
(a)



(b)



(c)



(d)

Figure 5. Lab-VIEW waveform of 2 stage Fractional-order Phase Locked Loop at (a) α=1, β=1 (b) α=0.4, β=0.4 (c) α=0.6, β=0.8(d) α=0.8, β=0.4.

In the above figures the phase responses of the FPLL have been taken at different α and β values and compared.

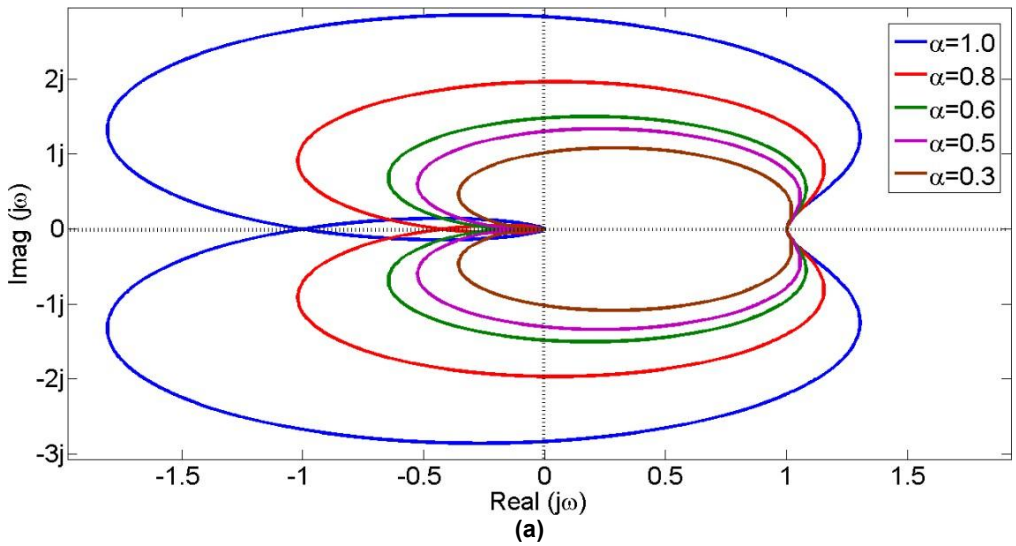
Table 3. LabVIEW data of FOPLL at variable fractional orders α and β.

Fractional Orders	Maximum peak (degrees)	peak time (n sec)	Settling time (n sec)
α=1.0, β =1.0	65°	5	50
α=0.4, β=0.4	55°	7	30
α=0.6, β=0.8	55°	6	40
α=0.8, β=0.4	72°	5	72

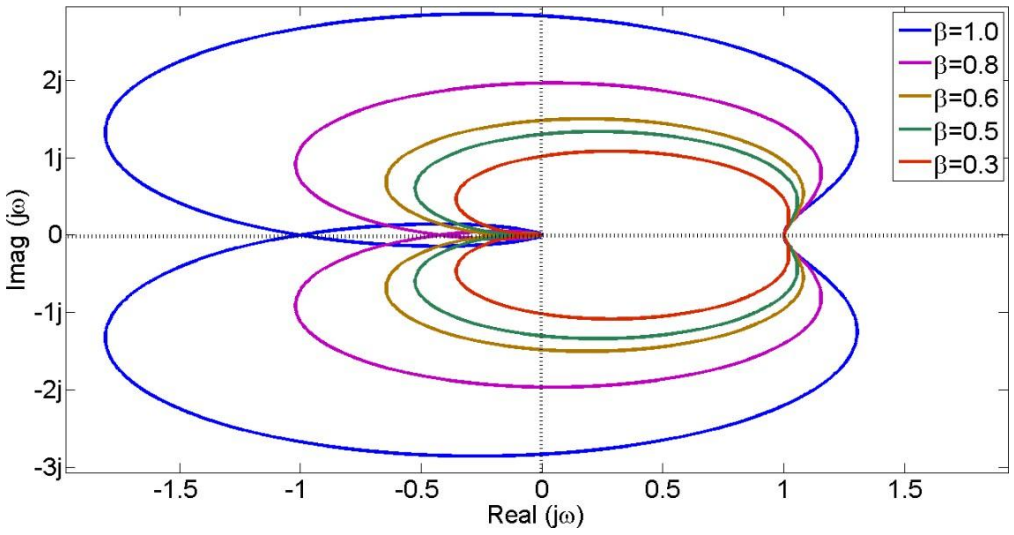
In figure (a) the response takes nearly 50 nsec to settle or become steady. Similarly, in figure (b) it takes 30 nsec to settle ,40 nsec and 72 nsec for figure (c) and figure(d) respectively. From the above data it has been found that at α =0.4, β =0.4 the required settling time is the least.

3. STABILITY ANALYSIS OF FOPLL

Stability analysis of the Fractional order PLL is carried out by making use of the fractional transfer function of the circuit in control domain and then evaluating its magnitude and phase mathematically in MATLAB. Then for each order of α and β the Nyquist plot is generated by making use of magnitude data versus the imaginary data.



(a)



(b)

Figure 6. Nyquist plot of fractional order PLL Circuit at (a) β constant i.e., 1 and α varying and (b) α constant i.e., 1 and β varying.

Stability of the closed loop system was found using Nyquist plot. We know if the critical point (-1+j0) lies outside the encirclement, the closed loop system is absolutely stable. Hence, it is quite evident that advancements could be done for the stability analysis of FOPLL. As interpreted from the Nyquist plot shown in figure.6, the entire circuit could be stabilized in future works by making use of any advancements.

3. CONCLUSIONS

Stability In this paper the performance analysis of the Fractional order phase locked loop (FOPLL) is being studied and it was characterized that, at the fractional orders α=0.4 and β=0.4, the FOPLL shows elite performance. Not only it has an improved response but also it ensures a better stability. A comparative analysis of MATLAB and LabVIEW shows a marginal behavioral change in the proposed system. As the initial condition and the approximation criteria is different for different simulation software.

REFERENCES

[1] *S. Huang, S. Liu and Z. Zhu, "A High-Resolution 2-GHz Fractional-N PLL With Crystal Oscillator PVT-Insensitive Feedback Control," in IEEE Microwave and Wireless Components Letters,* ***(2018)*** *vol. 28, no. 3, pp. 227-229.*

[2] *K. Biswal, S. Swain, M. C. Tripathy & S. K. Kar "Modeling and Performance Improvement of Fractional-Order Band-Pass Filter Using Fractional Elements", IETE Journal of Research,* ***(2021)****.*

[3] *D. Liao and F. F. Dai, "A Fractional-N Reference Sampling PLL With Linear Sampler and CDAC Based Fractional Spur Cancellation," in IEEE Journal of Solid-State Circuits,* ***(2021)****, vol. 56, no. 3, pp. 694-704.*

[4] *S. Swain, K. Biswal, M. C. Tripathy and S. K. Kar, "Performance Analysis of Fractional Order Sallen-Key High-pass Filter Using Fractional Capacitors," 2020 International Conference on Computational Intelligence for Smart Power System and Sustainable Energy (CISPSSE),* ***(2020)****, pp. 1-5.*

[5] *S. Swain, S. P. Thatoi, M. C. Tripathy, "Modeling and Performance Improvement of Multistage Fractional Order BJT Amplifier", International Journal of Engineering Science and Computing,* ***(2020)*** *ISSN 2321 3361 © 2020 IJESC, Vol. 10, issue. 2, pg.26596-26599.*

[6] *S.P Thatoi, S. Swain, M.C. Tripathy, "Design and Analysis of Fractional Order Transistor Amplifier", International Journal Of Engineering Research And Development, e- ISSN: 2278-067X, p-ISSN: 2278-800X,* ***(2020)*** *Volume 16, Issue 7, PP.25-33.*

[7] *K. Biswal, M.C. Tripathy, S. Kar, "Performance Analysis of Fractional Order High-pass Filter." Lecture Notes in Electrical Engineering (IEPCCT), Volume 630, pp:511-519, Springer, Singapore,* ***(2020)****.*

[8] *M.C. Tripathy, K Biswas, S Sen, "A design example of a fractional order Kerwin Huelsman- Newcomb bi-quad filter with two fractional capacitors of different order", Circuits, Systems and Signal Processing* ***(2010)****; 59:1586–1593.*

[9] *A. Soltan, A.G. Radwan, A.M. Soliman, "CCII based fractional filters of different orders," J. Adv. Res.,* ***(2014),*** *vol.5, no.2, pp.157-164.*

[10] *M.C. Tripathy, D. Mondal, K. Biswas, S. Sen, "Experimental studies on realization of fractional inductors and fractional order band pass filters", International journal of circuit theory and applications,* ***(2015)****, 43 (9), 1183-1196.*

[11] *A.G. Radwan, A. S. Elwakil and A.M. Soliman, "On the realization of second-order filters to the fractional domain", Journal of circuits and system,* ***(2009)****, vol. 18, No. 2, pp. 361-386.*

[12] *A. Adhikary, S. Sen, K. Biswas, "Practical realization of tunable fractional order parallel resonator and fractional order filters", IEEE Transactions on Circuits and Systems-I,* ***(2016)*** *63(8):1142–1151*

[13] *A. Adhikary, S. Sen, K. Biswas ''Design and hardware realization of a tunable fractional-order series resonator with high quality factor''. Circuits, System Signal Process.,* ***(2016)****, Vol.36, No.9, pp.3457-3476.*

[14] *K. Biswal, M.C. Tripathy, S. Kar, "Performance Analysis of Fractional Order Low-pass Filter." Lecture Notes in Networks and Systems (ICAC),* ***(2020)****, Volume 109, pp:224-231, Springer, Singapore.*